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# Disclaimer – Statements of Future State

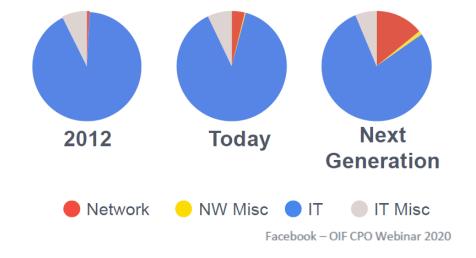
Material does not necessarily represent opinions of Microsoft and certainly cannot be construed as any form of commitment by Microsoft towards pursuing concepts described herein

long-haul DWDM long-haul DWDM **400G** DWDM 400G >100km >100km (400ZR) <100km (2021-)RNG RNG Optical Optical Ċore Core Core Core Hub Hub Hub Hub West West **400G** DWDM (400ZR)<100km Tier 2 Tier 2 Tier 2 Tier 2 **400G** DR4 <1km / row Tier 1 **400G** AOC ∕ rack <30m ToR 100**G** DAC <2m Microsoft Azure

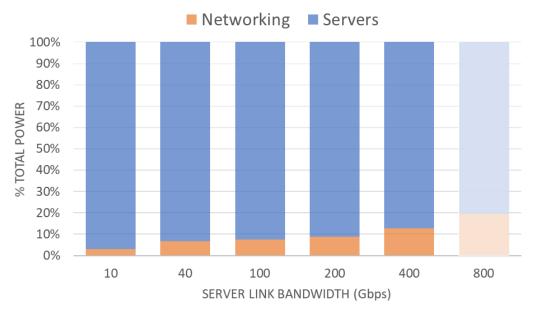
EPIC - Roadmap 2021 beyond 400G | 21 Apr 2021

#### Power limits future DC scaling

- Equipment power consumption at 400G is already problematic!
  - Switches projected @ 3x power of 100G
  - Optics projected @ 3-4x power of 100G
- Challenges power envelopes of facilities
- Uses power that could be generating revenue (lost server capacity)
- Costs \$\$\$ and not green
- Trajectory makes transition to >400G appear all but impossible



#### NETWORK COMPONENT OF DATACENTER POWER

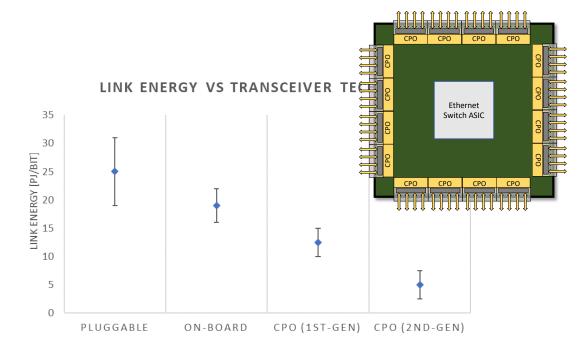


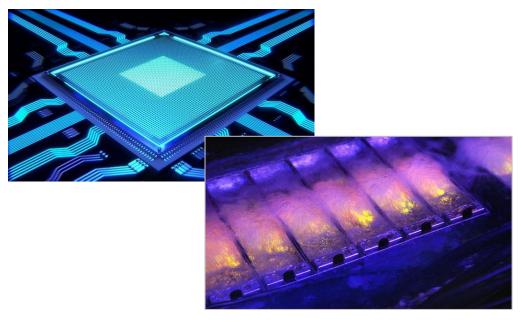


#### Possible Solutions

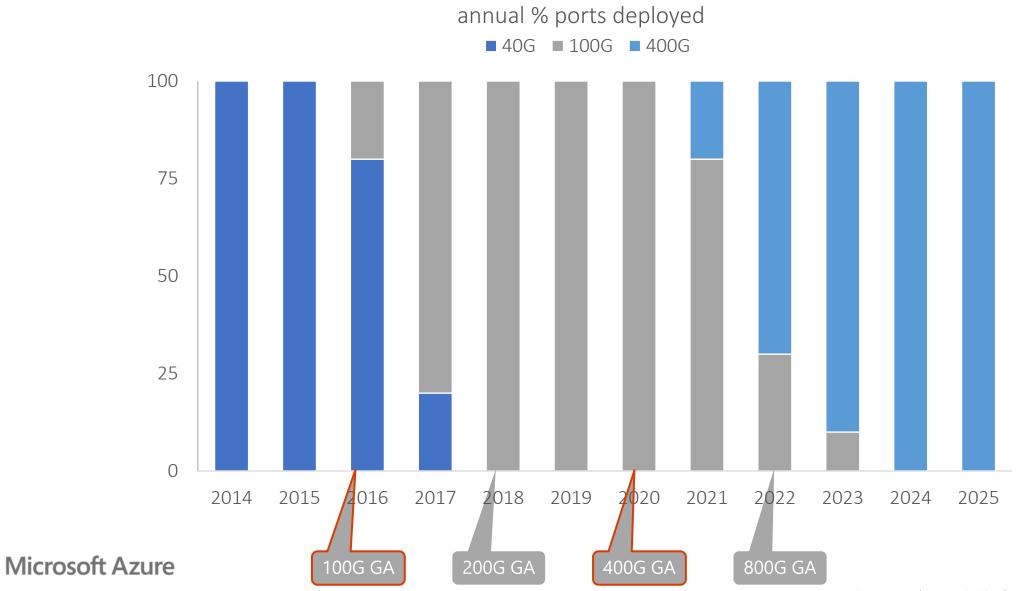
- Photonics
  - Co-Packaged Optics (CPO)
  - Novel optical approaches
- Network architecture + HW changes
  - Collapsed tiers with multi-homed NICs (fanning out horizontally)
  - Simplified forwarding requirements → cooler ASICs
  - Additional integration, e.g. encryption on switch ASIC
  - Liquid cooling

Takeaway: we can't just keep scaling link bandwidths... "next gen" systems will require all of the above

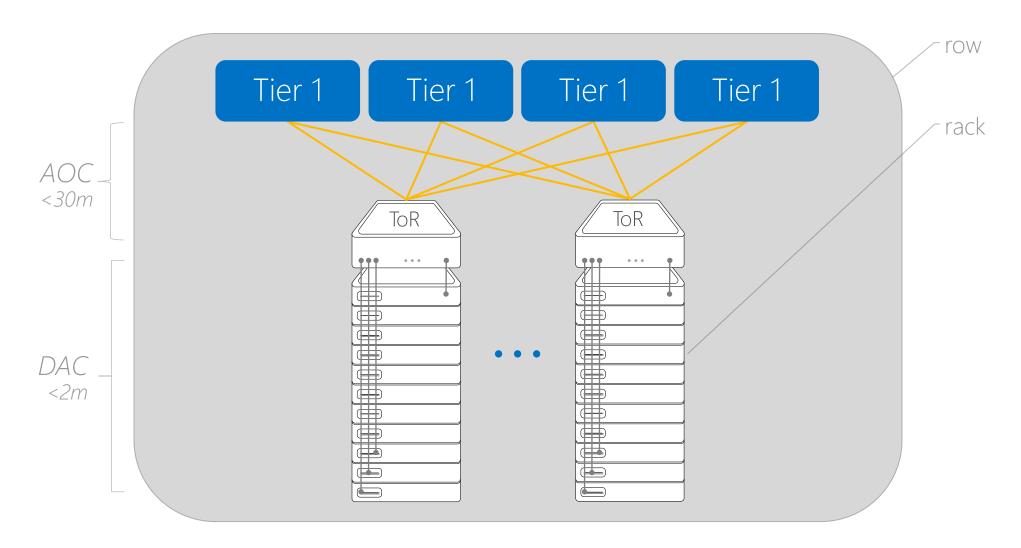




### Microsoft DC ecosystem technology life cycles

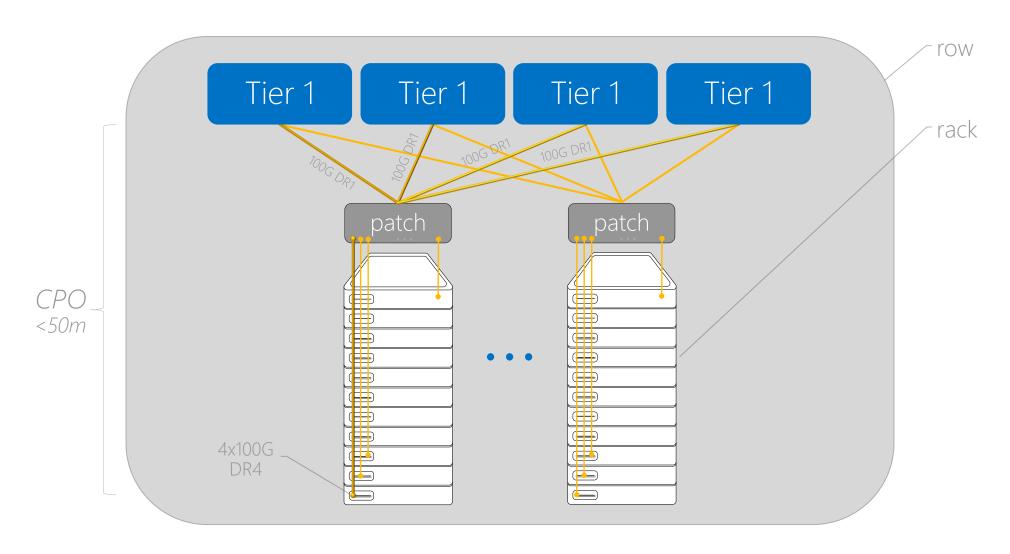


## Server-ToR-Tier1 topology



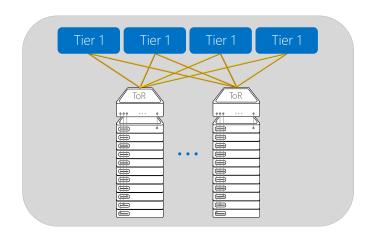


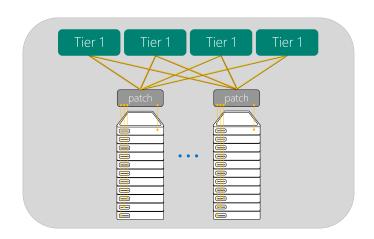
#### ToR bypass – multi-homed NIC





### ToR bypass efficiencies (100G lane speeds)





	Tier1-ToR-server	ToR-bypass
failure domain	ToR is SPOF for rack	no SPOF – multi-homed NIC
switch ASIC count	4X-8X	1X
switch space + power	baseline	reduced space and ~1/3 power
switch radix	can't leverage higher radix chips (stranded capacity at ToR)	leverages full switch radix
oversubscription	3:1 typical	fully non-blocking in row
reach limits	DAC < 3m; AOC < 30m	1m-2km <sup>+</sup>



#### Summary

- Power is the main limiter for "beyond 400G" data centers
- We can't continue to simply scale link bandwidths while building networks exactly as we do today
- Historical ecosystem life cycles would indicate we won't be ready for "800G" when the industry is (32x100G CPO will suit our needs better)
- 100G electrical lanes will be a foundational building block for powerefficient data center designs for the foreseeable future
- Future data center networks will require a combination of photonic innovation (e.g., CPO), optimized network architectures, and advanced hardware implementations



