

Flash Imaging Miniaturization

*Near-range / low latency detection
using 3D-stacked CMOS technology*

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2022, 2017



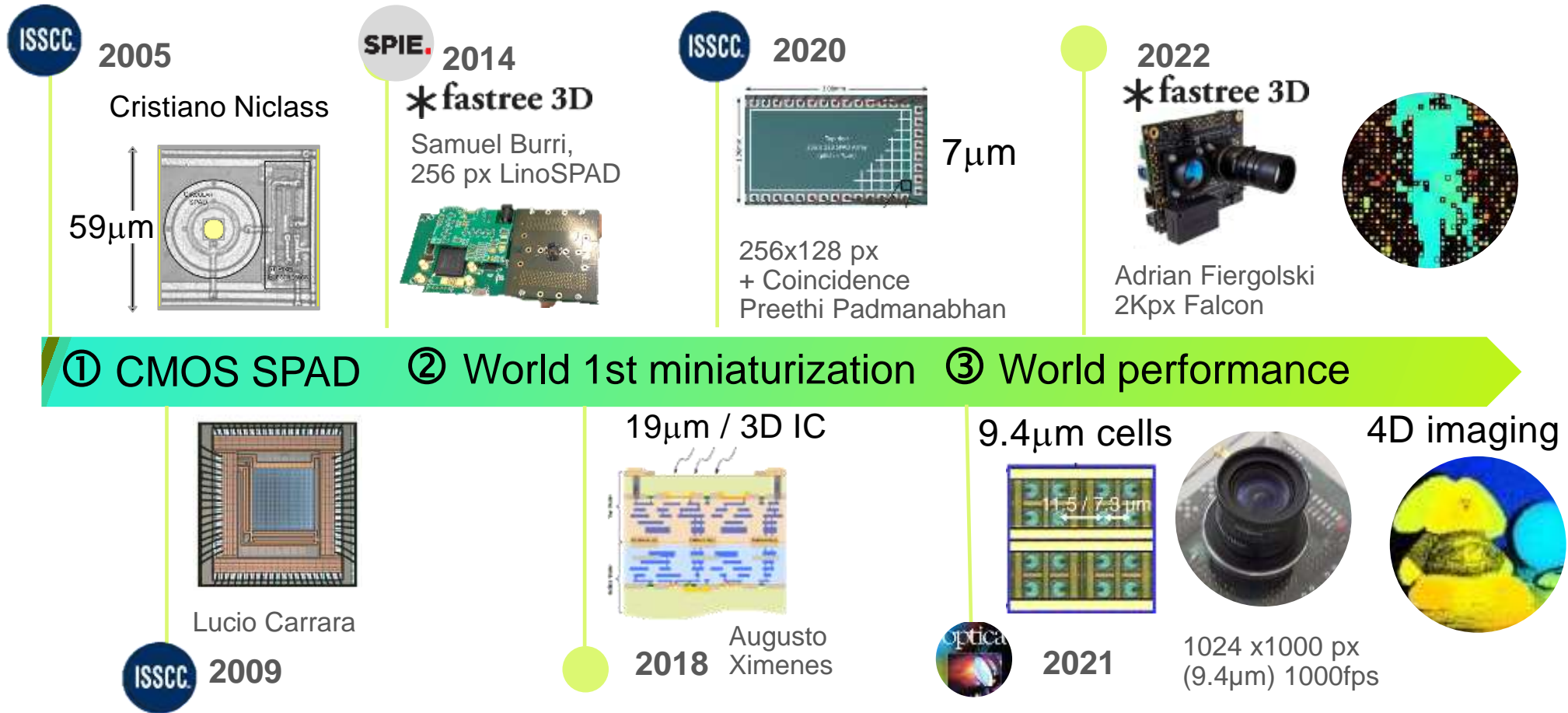
Fastree3D-Flash_LiDAR-miniaturization-V.1.pptx



Outline

- Fastree3D and EPFL collaboration history
- Flash LiDAR miniaturization module
- CMOS SPAD miniaturization trends
- 3D wafer-level stacked circuits evolution and performance
 - EPFL prototypes with TSMC
- Towards software-defined Flash LiDAR
 - Integration plan, optimization points
- Value proposal

Fastree3D / EPFL collaboration history



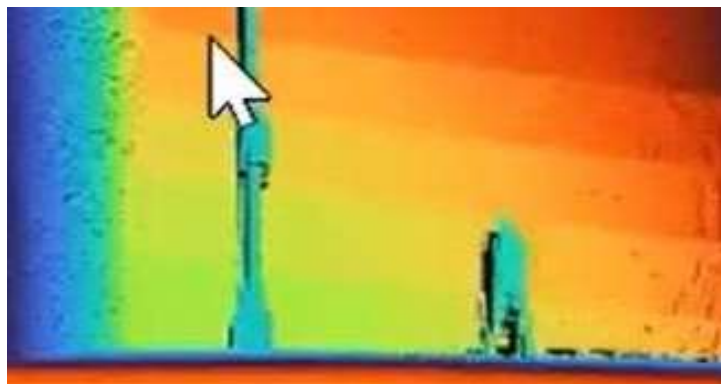
* ISSCC is the "Olympics of Semiconductor industry", SPIE is the world's #1 photonics association

EPFL aqua lab, R. Charbon 2021

Flash LiDAR miniaturization approach

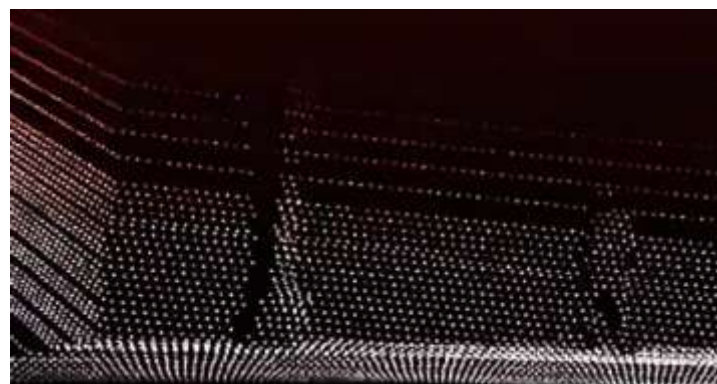
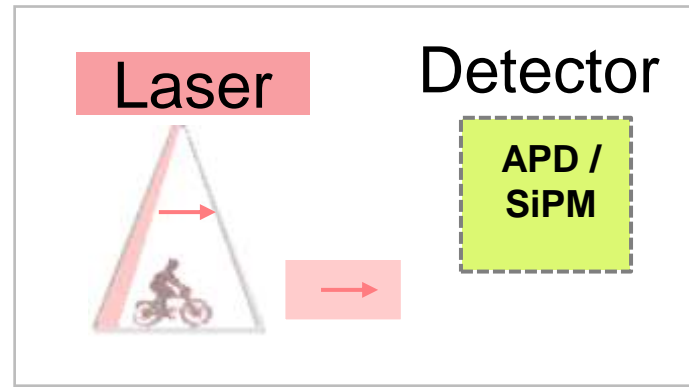
Animation

Flash



Images acquired from the web for illustration only

Scanner



Flash

- High 2D pixel count
- Photon counting
- Fast acquisition (MHz)



- Lower optical power

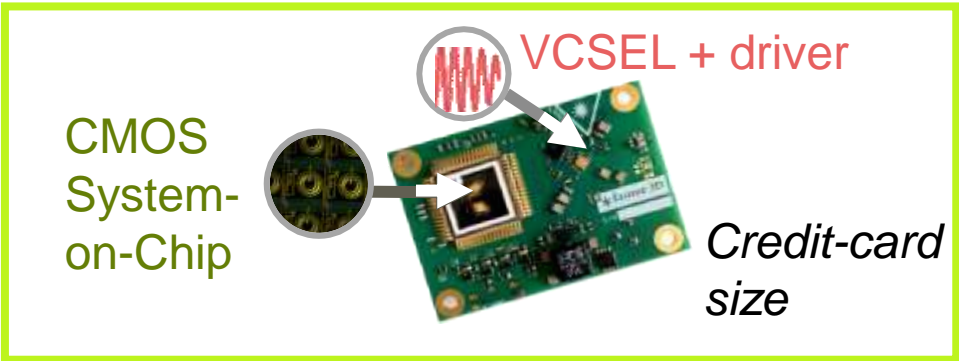
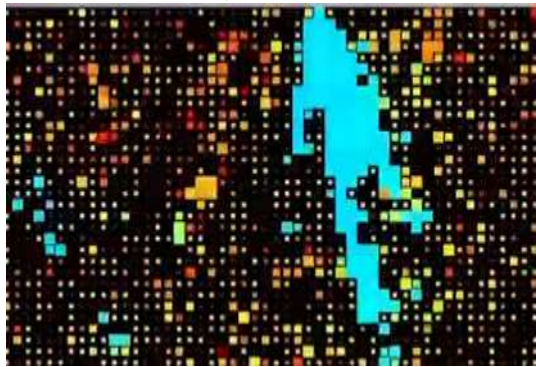
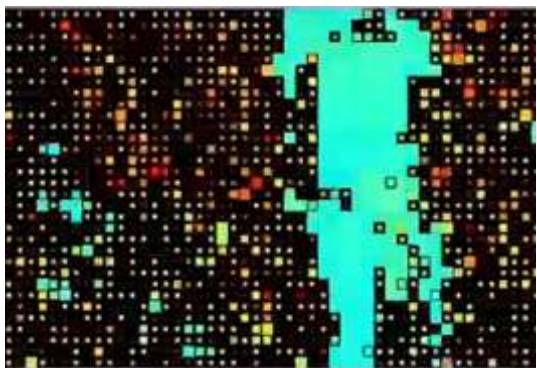
Digital chip



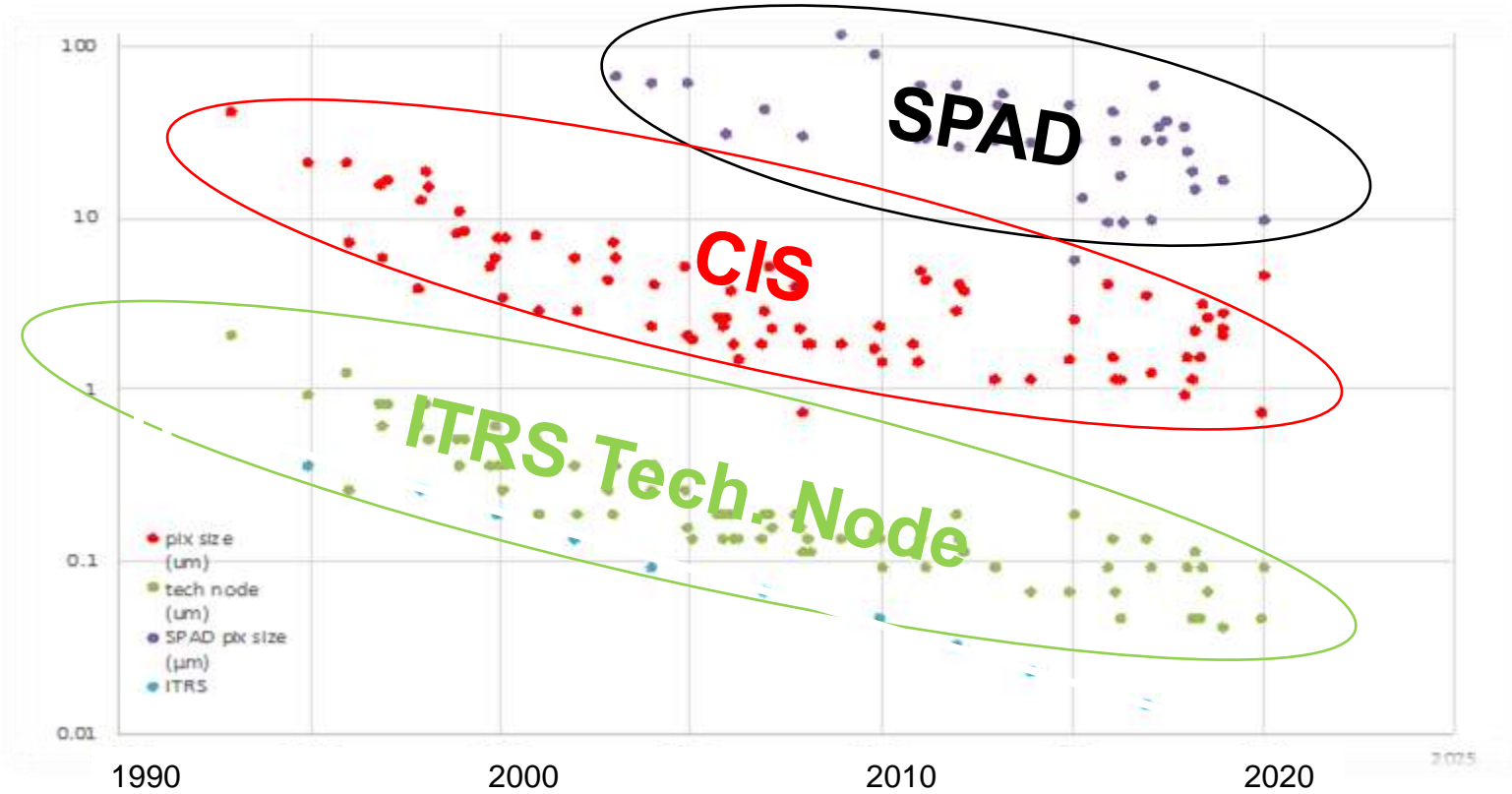
- Cost-effective implementation
- Software-defined

Flash LiDAR module miniaturization

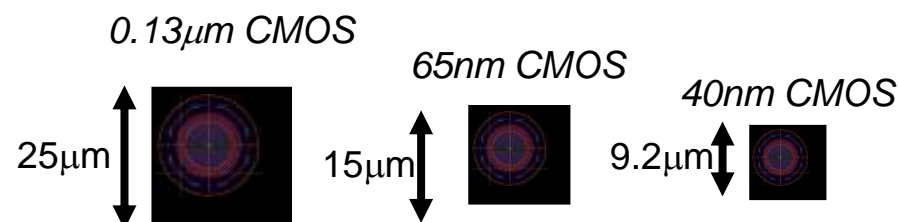
- ✓ Software-defined
- ✓ CMOS SPAD detector
- ✓ Flash illumination (VCSEL)
- ✓ Range 40m @ 10%r, 60klux



CMOS SPAD miniaturization trends



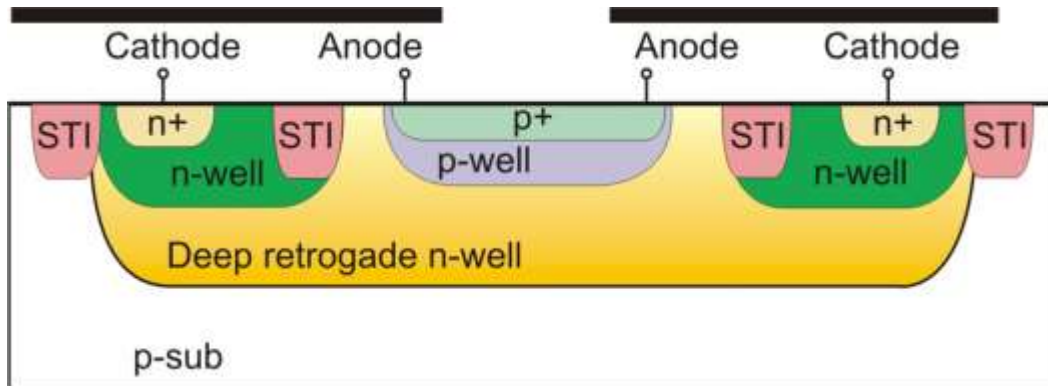
- Delays reasons
 - High voltage (older nodes support)
 - Guard rings
 - Lack of backside illumination process
 - Lower production volume
- Evolution
 - Low pitch
 - High fill factor
 - 3D-IC high performance



Source: Albert Theuwissen, Harald Homulle, Edoardo Charbon

From monolithic to 3D stacked circuits

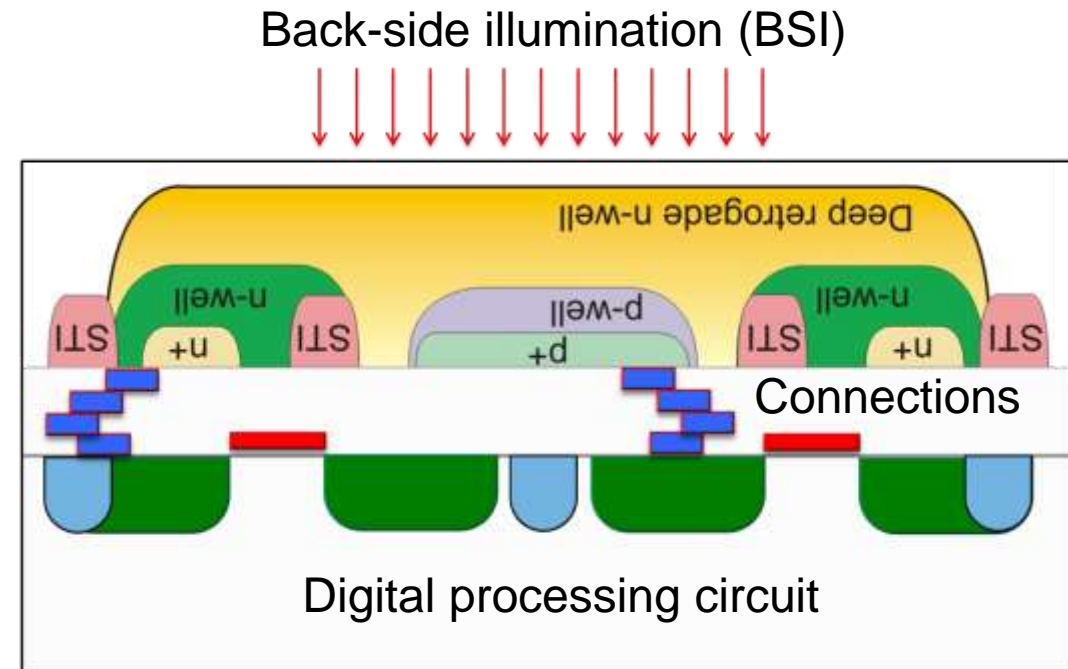
Monolithic implementations



- ✓ Simple electronics
- ✓ Lower costs

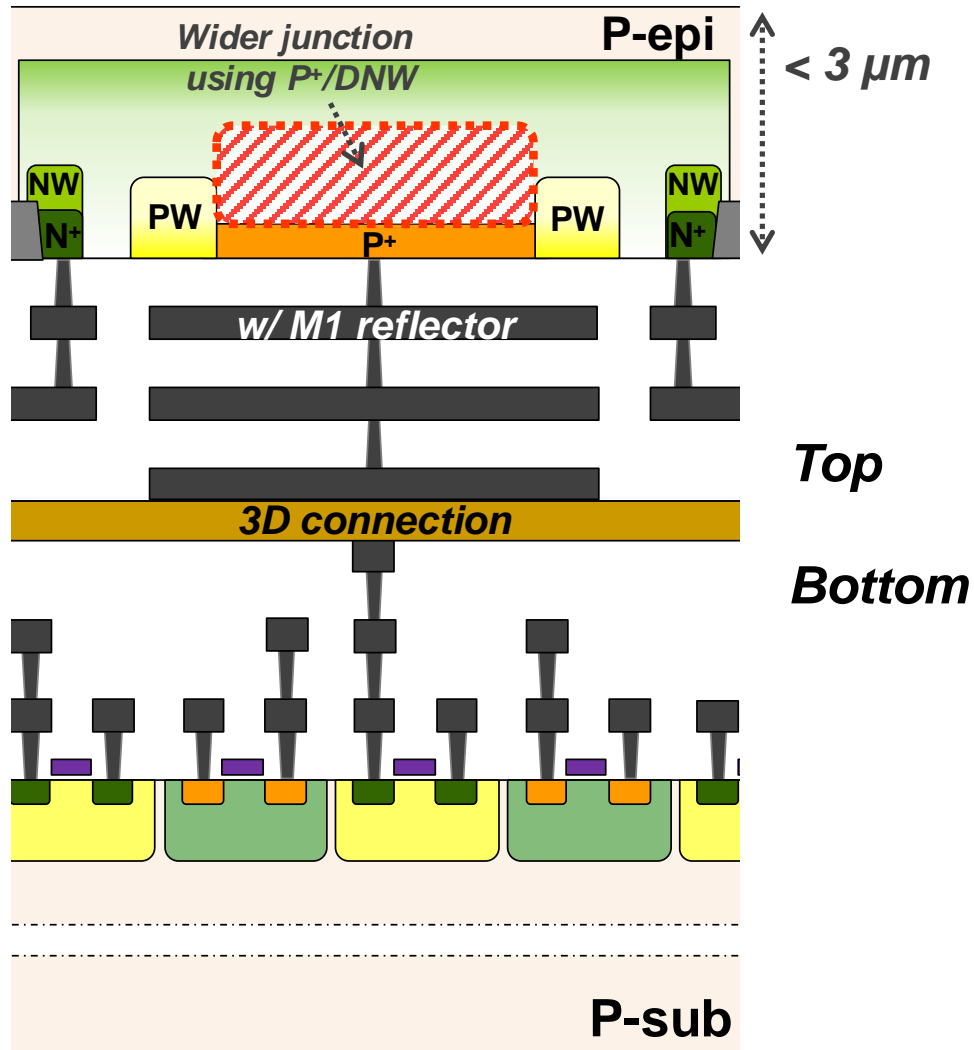
Sources : David Stoppa, Richard Henderson (schematics)

3D-stacking at wafer level



- ✓ Fill factor increase → sensitivity improvement
- ✓ Smaller pitch → higher pixel count
- ✓ Optimized CMOS for electronics → performance

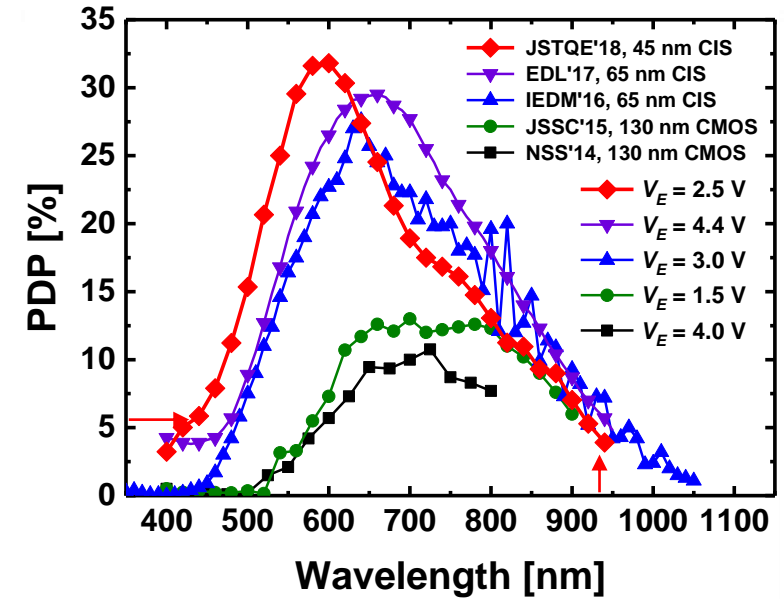
3D wafer-level stacking evolution



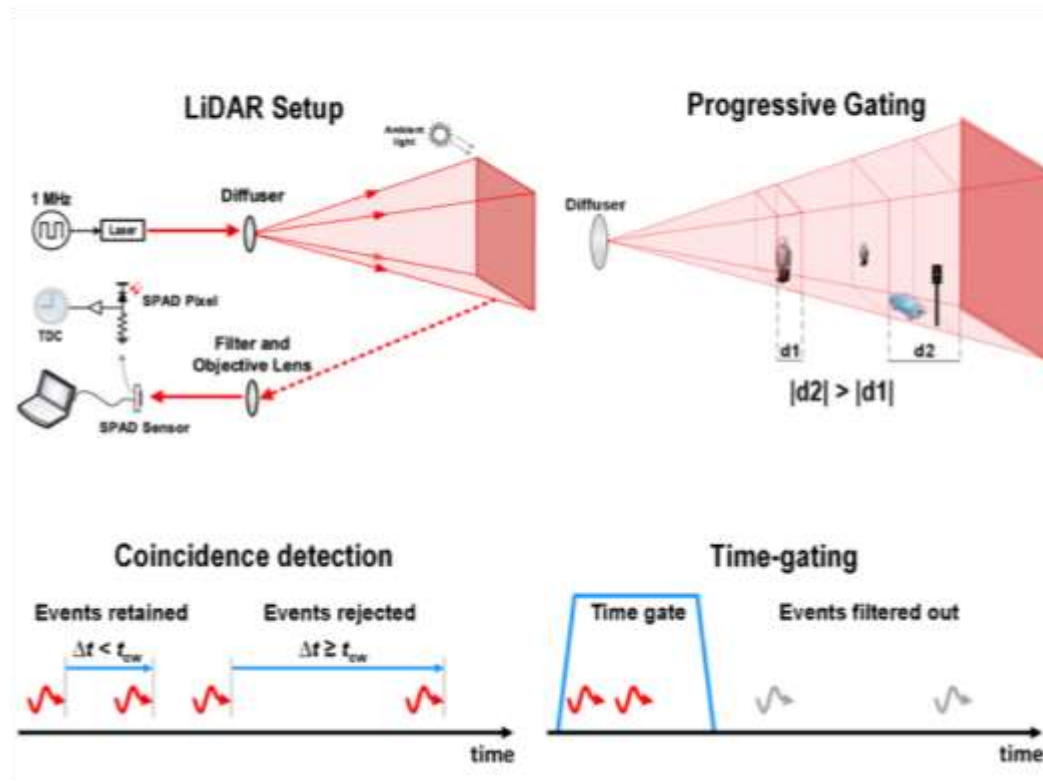
- SPADs (TSMC 65nm)

- TSV-less connections

- Electronic circuits (TSMC 45nm)
 - Quenching & recharge
 - Masking, region of interest
 - TDC (low power coupled oscillators)
 - Digital processing, coincidence management



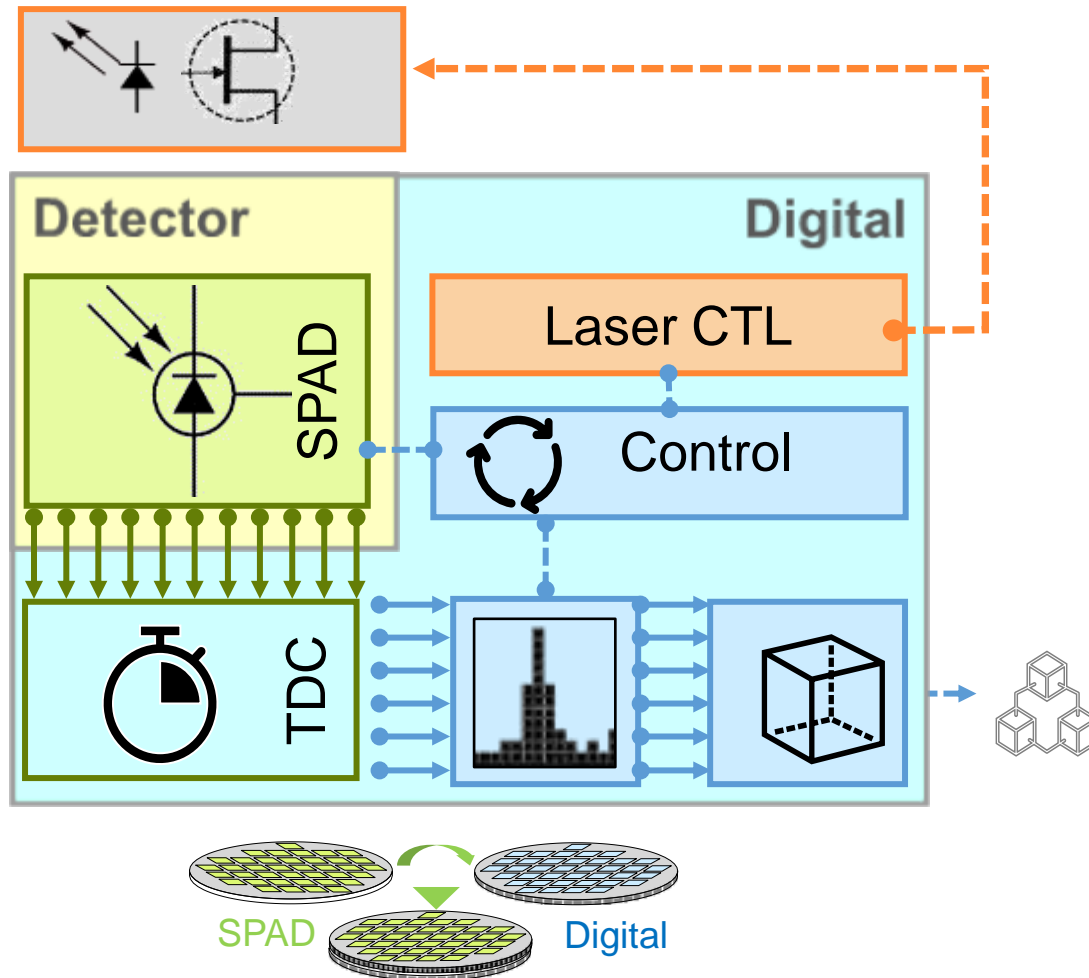
3D-stacking performance improvement



- Coincidence detection
 - 8x16 clusters
 - 7-level t_{CW} 500ps-2.2ns
 - Sunlight rejection
- Adaptive gating
 - 6 progressive ranges
 - 1.3ms exposure
- Interference suppression
 - SNBR increase >31dB

Source : Padmanabhan et al. A 256 x 128 3D-Stacked (45nm) SPAD FLASH LiDAR with 7-Level Coincidence Detection and Progressive Gating for 100m Range and 10klux Background Light", IEEE ISSCC, 2021

3D-IC software-defined implementation



- High-resolution detection
 - Lower pitch size $< 7\mu\text{m}$
 - Detection efficiency, gain $> 10^6$
 - 256×64 - 256×4 SPADs
 - Global shutter
- Hybrid Cu-Cu wafer bonding
- Digital processing & control
 - Time-gating
 - Coincidence for sunlight suppression
 - ToF processing
 - Adaptive illumination and RoI
 - Lower cost / pixel

Software-defined Flash LiDAR

Technology integration

① Large SPAD array



② Sunlight / interferences



③ TDC resolution / power



④ Digital 3D-IC

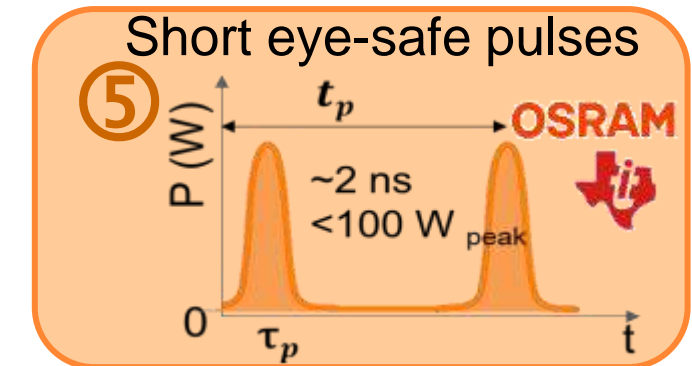
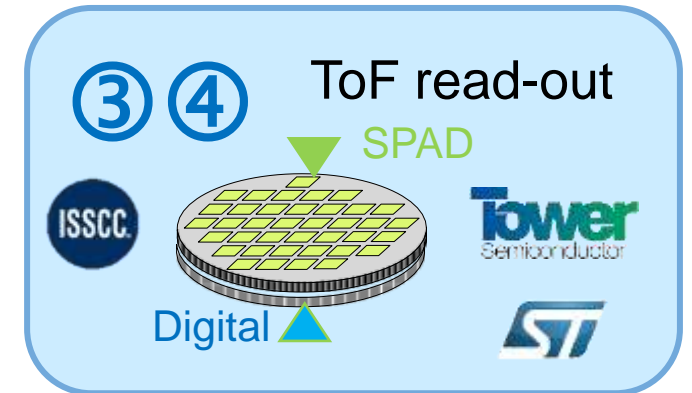
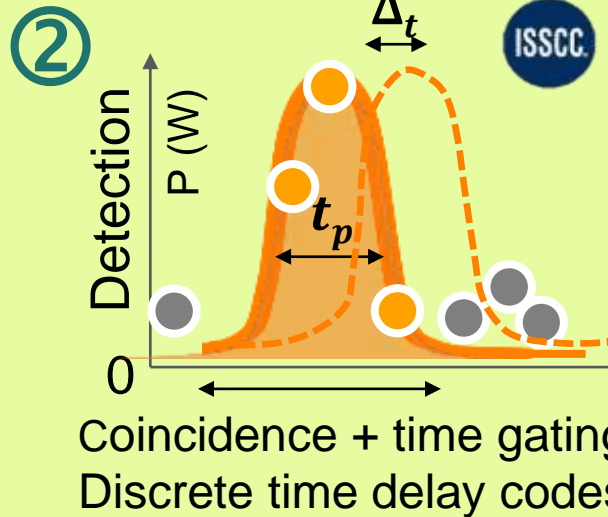


⑤ Laser eye-safe power



Real-time control

① Resolution scaling
1 Mpx 7 μm



Software optimization in real time



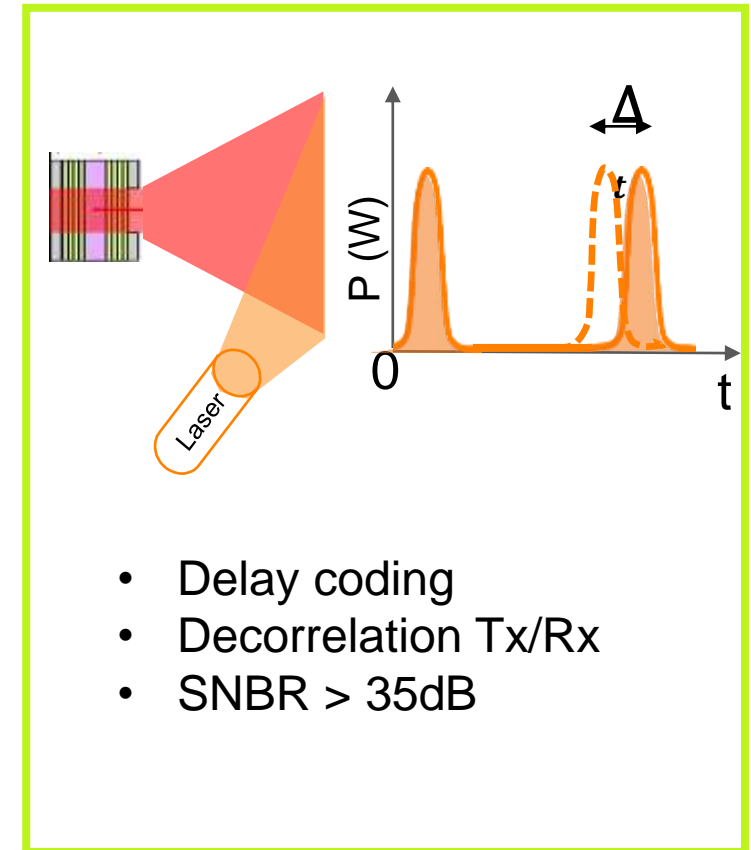
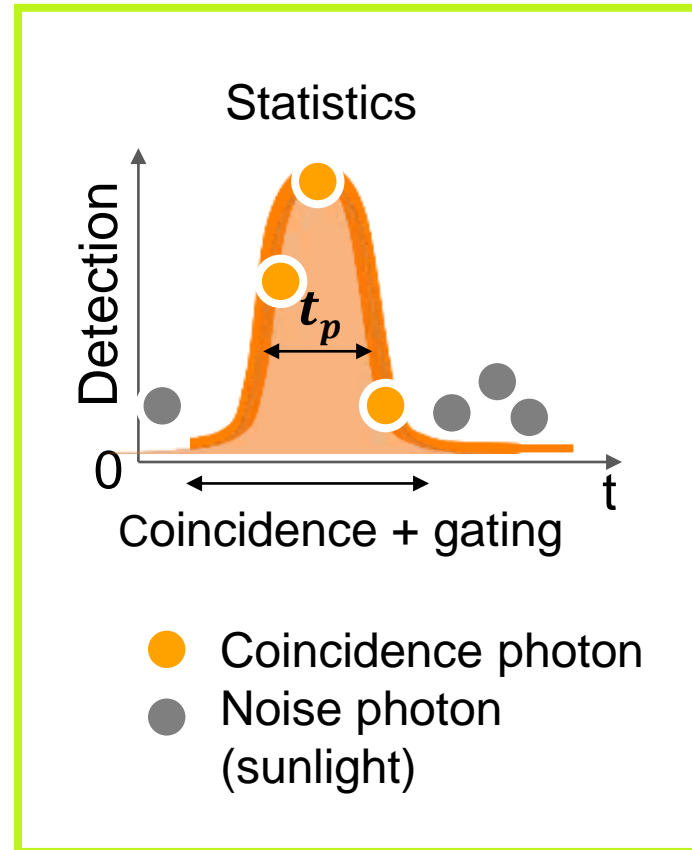
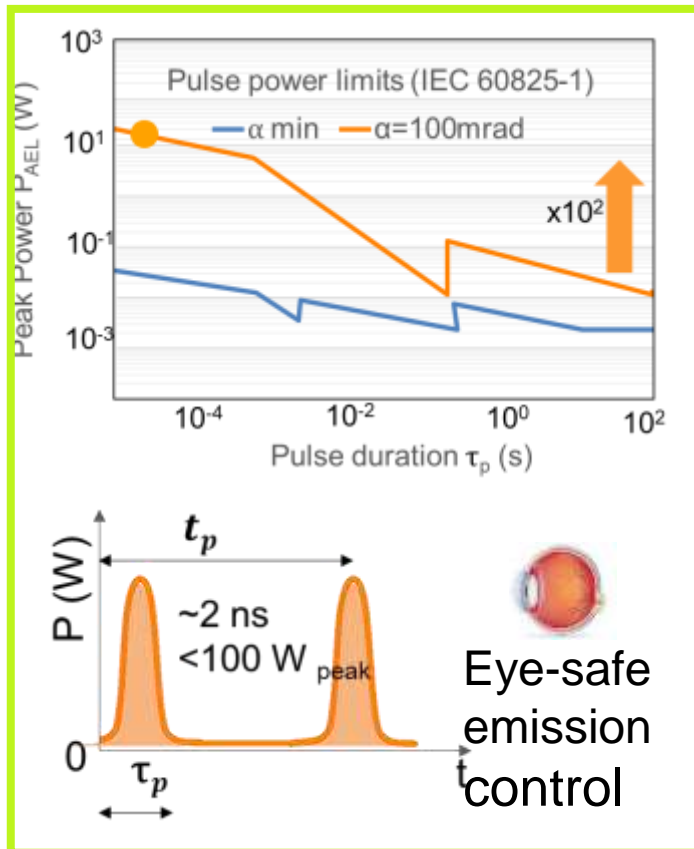
Illumination
to 50m



Sunlight
removal



Interference
removal



Software-defined Flash LiDAR value

Fast

Motion sensing for **emergency collision avoidance**



Lowest latency

Safe

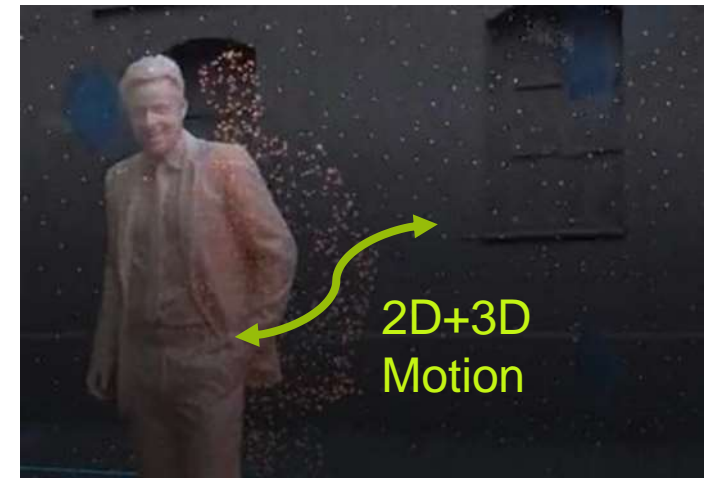
Low false detections under adverse lighting conditions



Quality control

Smart

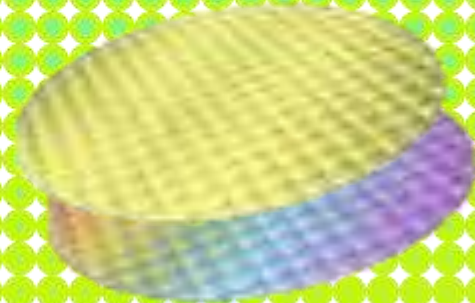
3D + 2D **actionable information** for effective sensor fusion



Edge computing

Thank you

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Automotive
safety



Autonomous
vehicles

