

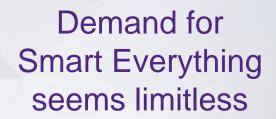
#### Change Occurring in Many Markets









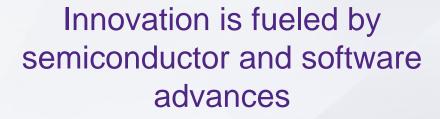


















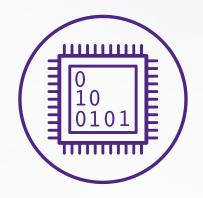


Driven by fusion of big data, massive compute, and machine learning

#### Macrotrends



Software Drives
Differentiation

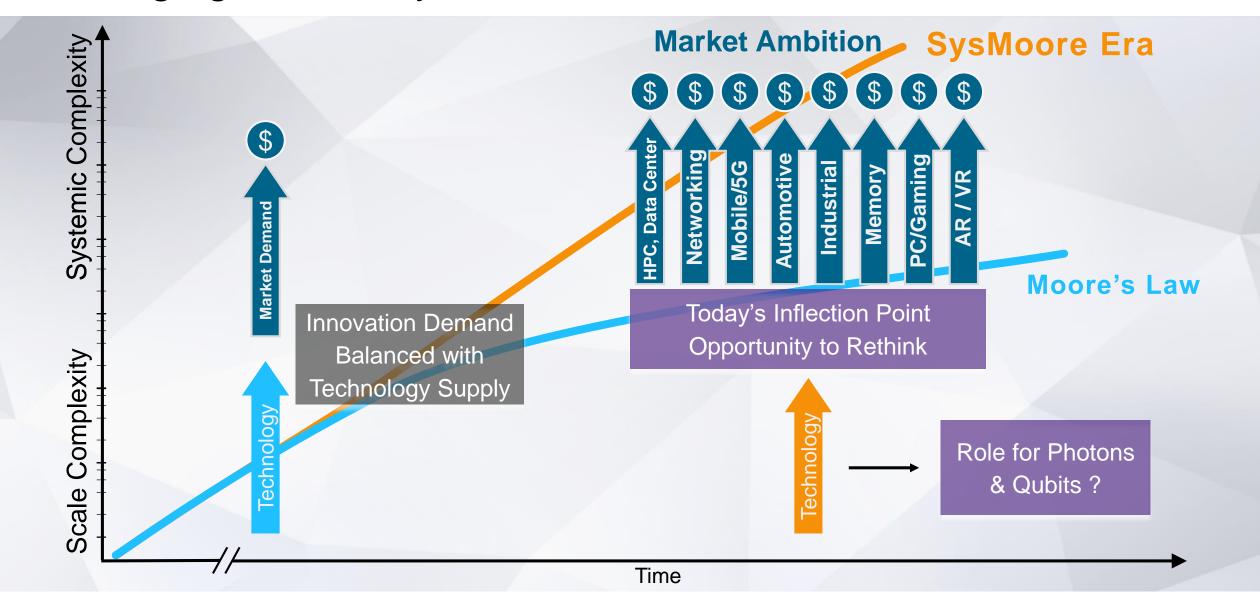


Chips Make This Possible

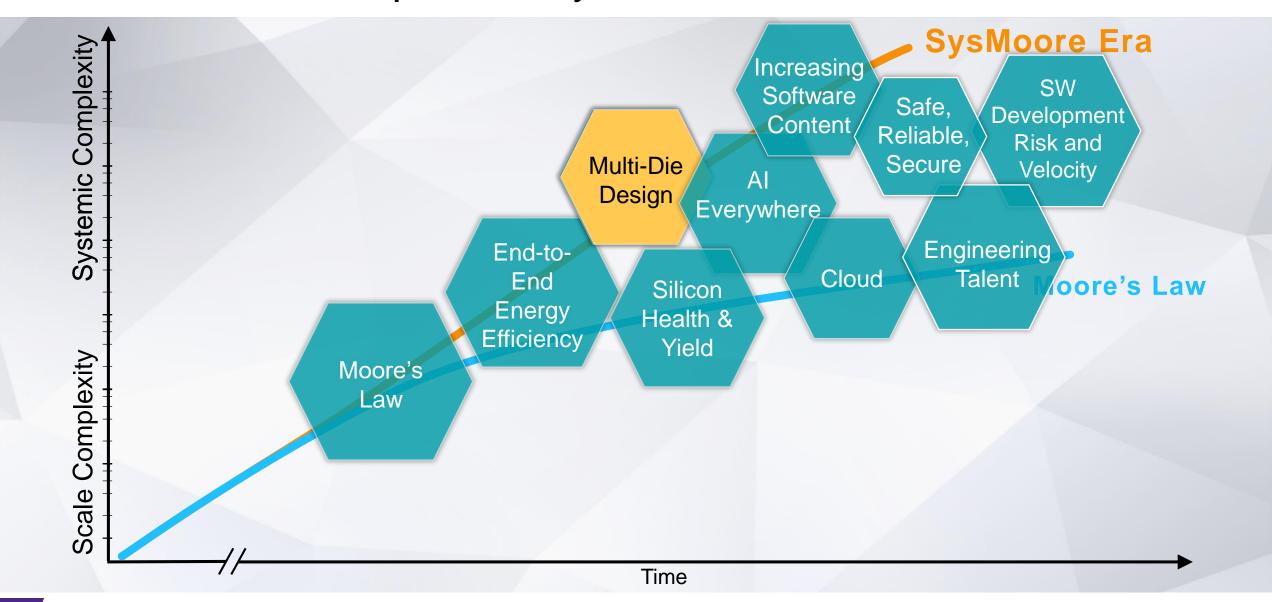


Optimized Software & Chip Development Key to Success

#### **Changing Market Dynamics**



#### Techonomic Disruptors in SysMoore Era

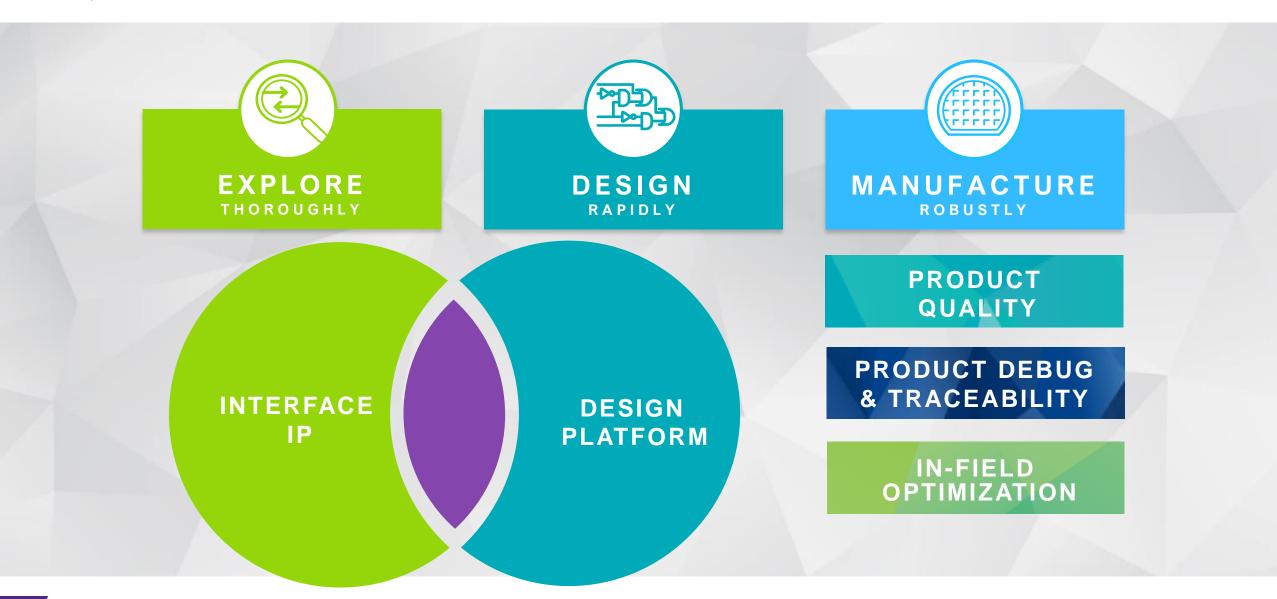


System-of-Chips

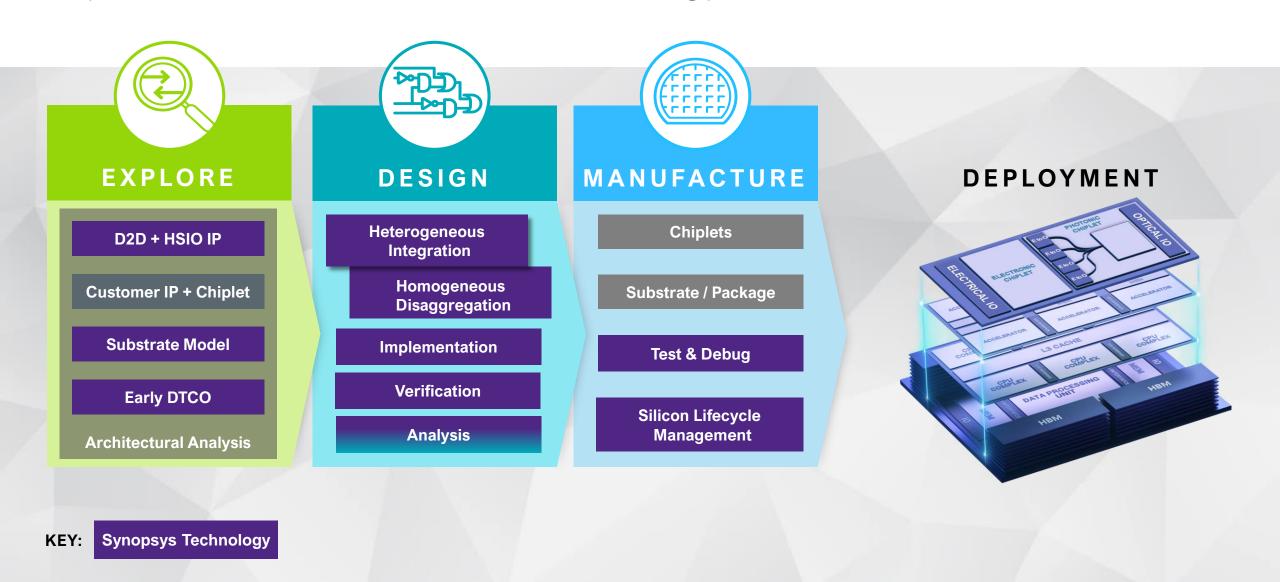
SYNOPSYS°



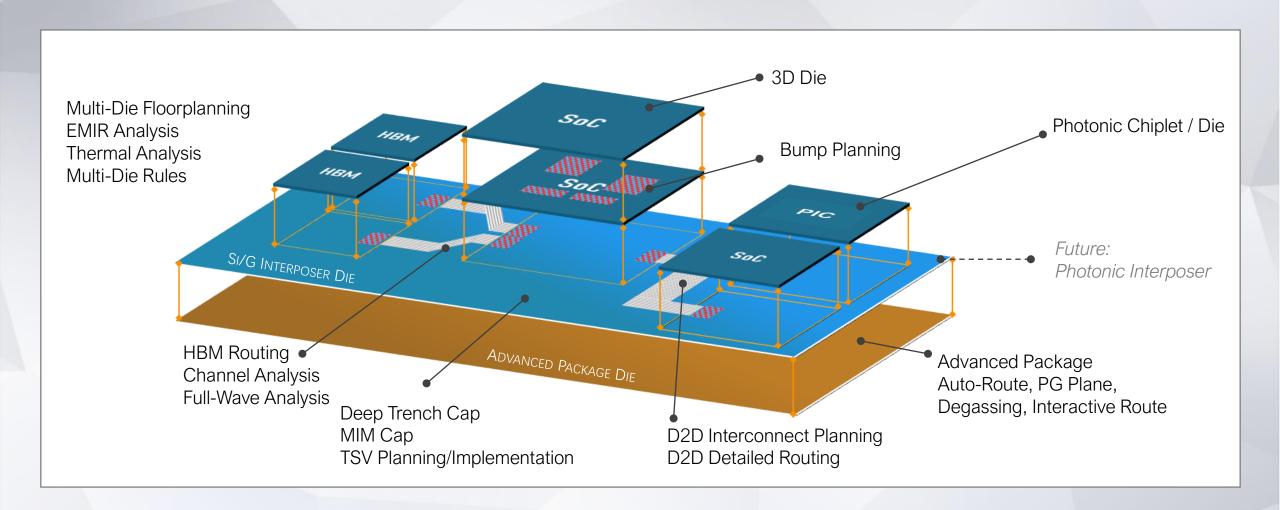
#### System-of-Chips Innovators' Journey



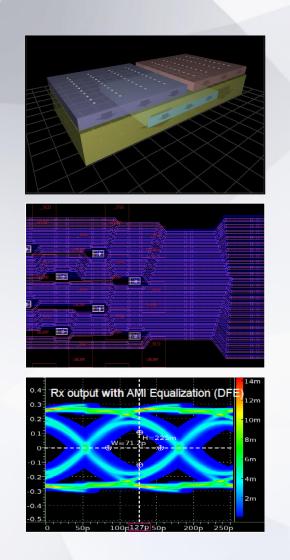
#### System-of-Chips EDA Methodology

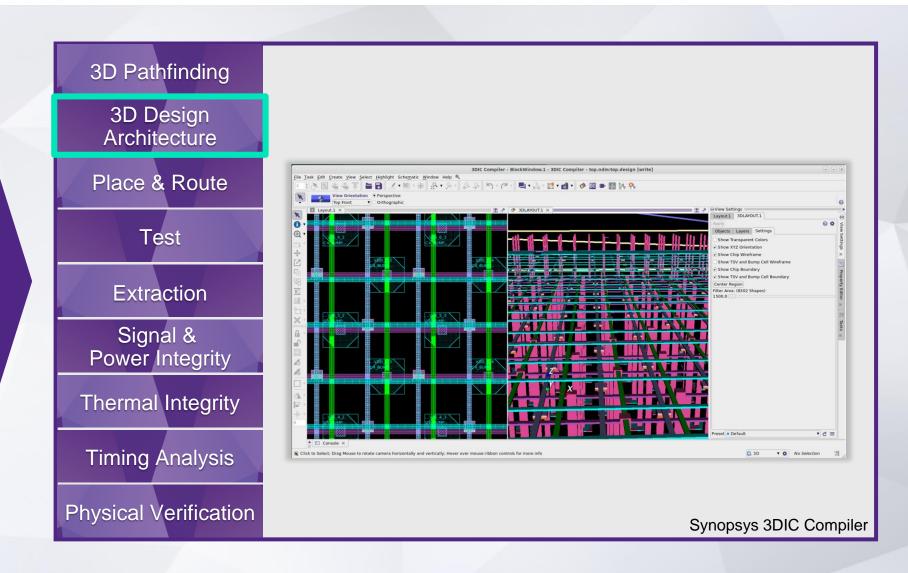


#### Multi-die / Multi-domain System Implementation

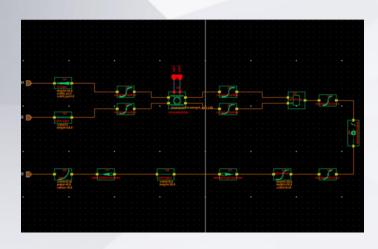


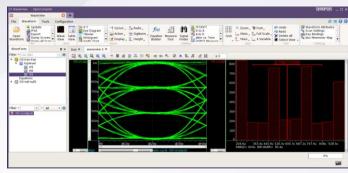
#### 3D Design Platform

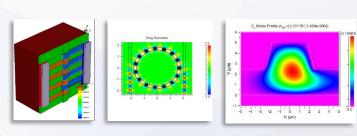


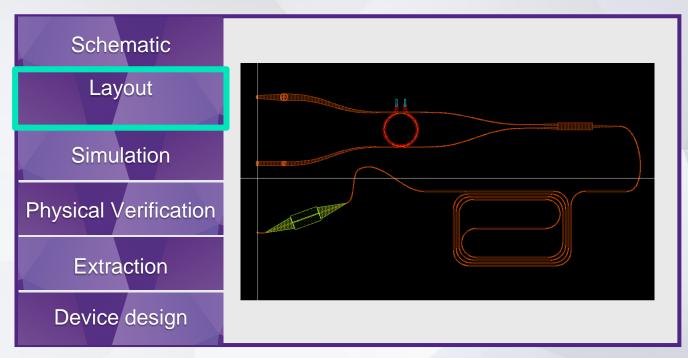


#### Electronic & Photonic IC Co-Design Platform









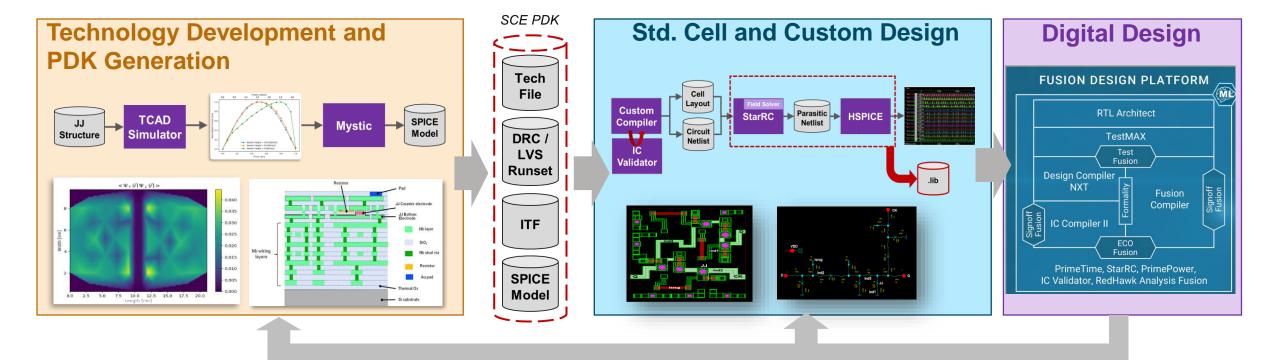
Synopsys OptoCompiler, OptSim, PrimeSim, Photonic Device Compiler, IC Validator, StarRC

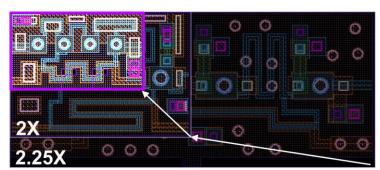
#### Quantum Computing based on Photonic ICs



#### Superconducting Electronics (SCE) TCAD & EDA Flow Developed Under The IARPA sponsored SuperTools Program:

A Comprehensive Flow for DTCO of Superconducting Technologies and Circuits



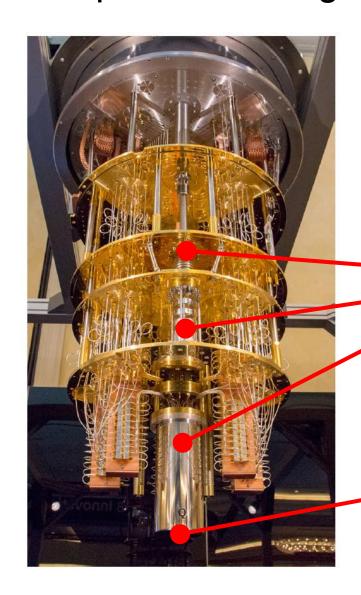


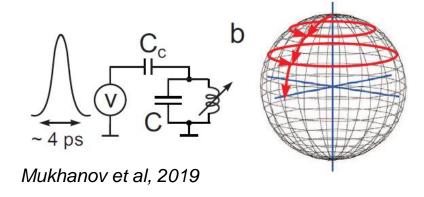
**DTCO** flow supports scaling of SCE technologies to achieve higher functionality

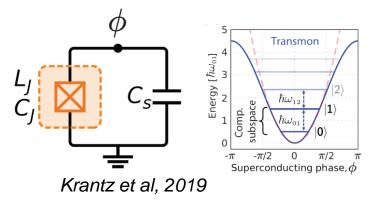


Provides foundation for new solutions to address **Quantum Computing** superconducting designs

## Synopsys Activity: Extend SuperTools Flow to Support Optimization of Superconducting-Based Quantum Hardware

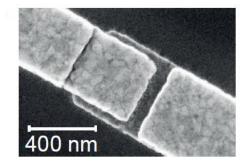


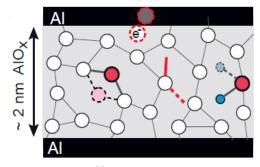




Design of superconducting and cryo-CMOS qubit control and read out interface circuits

Design, noise modeling and manufacturing optimization of superconducting qubits





Muller et al, 2019



### Thank You



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Silicon to Software™