Bay Photonics

- Packaging Photonic
- Components & PICs for
- Quantum Technology 2.0



Andrew Robertson

Nov 2022





Bay Photonics Products & Services



- Downstream photonic semiconductor (chip) processing
 - Die attach & wirebond, PIC packaging, co-packaging, hermetic (e.g. butterfly, TO)
 - Optical & electronic interface design & simulation, thermal control
 - Manufacturing process development to enable transfer to volume manufacturing
- Founded 2007, comprising former Nortel Networks & JDS Uniphase engineers
- Many decades of industrial optics & photonic packaging experience



Bay Photonics Location & Heritage boy photonics





2020s EPIC Centre built
 Electronics & Photonics Innovation Centre

- 1950s STC builds factory
- 1980s worlds first fibre optic undersea cable systems
- 1990s Nortel Networks site employs 6000
- 2000s II-VI/Coherent, SIFAM, Lumentum, Spirent, G&H, Prior Scientific, Palomar



EPIC Technology Meeting on Electronics & Photonics – Two Sides of One Coin – Munich Nov 22

Manufacturing Process Development





Palomar 3880 die bonder





Palomar 9000 wedge bonder

AMADA Weld Tech hermetic seam sealer

Why does Quantum matter?



- Transformative change across multiple sectors
- Quantum Computing
- Quantum Secure Comms
- Quantum Sensing & Timing
- Quantum Imaging



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Quantum & PIC Collaboration Partner

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PACKABLE PIC



Innovate UK PACKABLE (IUK 104511) AQUASEC (IUK 104615) **SIDEWINDER** SIDEWINDER (IUK 133979) ECL SPLICE (IUK 106174) SPIDAR SPAD QFOUNDRY (IUK 48484) ARRAY AIRQKD (IUK 45364) Copper Tungsten SPIDAR (IUK 44835) HIQED (IUK 10001572) REDEEMA (EUROSTARS) PADME (IUK 10031438) Q-PODS (IUK 10032014) PCB bottleneck to minimise ground plane and FR4/Prepreg thermal feedback Q3MD (IUK 10032009) Videned and deepened with 4 M2 fixings available. SPLICE LIDAR TRANSCEIVER

Photonic Semiconductor Packaging



- Mechanical (strength, mass, shielding, fixturing etc)
- Electronic (current, RF, ESD, etc)
- Thermal (high power, low temperature, temperature stability, cryogenic)
- Environment (N₂, vacuum, hermetic)
- Optical (transparent material with characteristics to match other requirements!)

Quantum semiconductor packaging "divergence"

Semiconductor

Application	General Packaging Requirements			
	Wavelength	Environment	Heat dissipation	Minimum operating temperature
Computer CPU	non optical	Non- hermetic	High	-40C
Telco	"Colourless" Wideband	Non- hermetic	Low	-40C
LIDAR	Eye-safe	Non- hermetic	High	-40C
Quantum Technology	Narrow band (visible to IR)	Hermetic	High	-50C to cryo

Drive to Low cost

"Leveraging Telco/Consumer Electronics"

🗸 "Volume"

New optical Tx (*+ve*) margin only realised after 12 months of production and > 10000 units per month

Photonic Integrated Circuits



• Mainstream media view of "quantum chips"













PIC Reality



- No one material will do all functions
 - Need chip-to-chip optical interface
 - Not fibre
 - Electrical & optical chips need interfacing
- Low temperature operation
 - Vacuum
 - Cryogenic
- Higher & higher electrical I/O count
 - 10s of thousands for processors
- Light needs to get out of package
 - Transparent packaging
 - Mode field conversion, fibre optics





Photonic considerations



- Wavelength
- Optical performance expectations (IL, WDL, TDL, PDL)
- Number of optical I/O
- Edge vs surface coupling
 - Surface coupling allows wafer level testing
- Mode conversion waveguide tapers
 - Optical model?
 - Mode field measurements, far field measurements?
- Fibre array
 - Made up of "strands" consisting of 12 fibres, not arbitrary!
- Optical feedback restrictions
 - AR coatings, fibre lens designs, optical windows
- Power vs stability trade off

SPAD (QFOUNDRY)



commercial trial of

quantum secured communication

BT and Toshiba

launch first

services.

Written by BCC.

April 28, 2022

Member New



- Quantum emitters & detectors for fibre communication
- Fibre coupled SPADs
- Low temperature, -50C operation
 - Optimum TEC performance in vacuum
 - Standard telco is N₂
 - Standard welding machines do not seal in vacuum
 - Bay developed vacuum process for butterfly type packages



Vacuum Performance

- Average reduction in temp 5C to 7C
- Efficiency of TEC increases by ~15%

Virtual of



EY becomes first commercial customer to connect quantum secure data transmission between its major London offices.

Wednesday April 27, 2022

London, England and Japan – At an event held at BT Tower yesterday (Tuesday 26th April), BT and



QFoundry SPAD QFE1A4 vacuum butterfly package

SPAD (AIRQKD)



- "Standard" packaging
- Low temperature -40C operation
 - Optimum TEC performance in vacuum
 - Projection welding machines do seal in vacuum



AIRQKD CONCEPT

bay photonics

Advanced Photonics Assembly and Packaging



- Devices reached -40C
- Best performance -45C



AIRQKD SPAD TO8 Commercial in confidence

AIRQKD package performance

SPIDAR SPAD Array





- Quantum based LIDAR
- Needs electrical connection ROICs
- To achieve performance, -40C to -50C
 - Sealed under vacuum, hermetic
 - Hybrid housing TEC on high thermal conductivity material brazed insert

with 4 M2 fixings available.

- 300+ pin out electrical connections
- Optical window







2x16 test SPAD array with ROIC confidence

PIC flexibility is packaging challenge















- Manual die & wire bonders
- Piezo controlled sub-micron alignment stages
 - Pitch & yaw
 - Rotation (PM)

QUANTUM PROBLEMS



- Test, measurement & assembly
 - How do you test the performance of a single photon emitter?
 - How do you measure the wavelength of a single photon emitter?
 - How do you optimise transmission in a system with single photons?
- Optical component performance
 - Interact with the real telecoms network and your single photons will be lost! Even optical fibre has a loss.
 - To date QKD demonstrators are point-to-point
- The classical world
 - How do you filter out the sun in free space quantum comms?

Future enabling tech - optical

- Additive 3D Nanofabrication
 - Two-photon polymerization (TPP)
 - Inter-chip connectivity
 - Optical componentry
 - Free form lenses & mirrors
 - Several companies developing workstations



Source: KIT/Vanguard Photonics







Future enabling tech



Karlsruhe School of Optics & Photonics (KSOP) KSOP 1.869 followers 1w . 3

+ Follow

KSOP members Yilin Xu, Christian Koos and their colleagues wrote a paper about 3D-printed facet-attached optical elements for connecting VCSEL and photodiodes to fiber arrays and multi-core fibers. In their paper they d ...see more



3D-printed facet-attached optical elements for connecting VCSEL and photodiodes to fiber arrays and multi-core fibers - Multicore optical fibers and... arxiv.org • 2 min read

CCO Torsten Vahrenkamp and 67 others 4 reposts

Comment

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Fig. 5. Three-channel transceiver module implemented on a small form-factor pluggable PCB. Three Tx VCSEL 1, 29, and 3 and three Rx PD 4, 5, and 3 are connected to three cores of the associated MM-MCF.

Wafer level PIC fabrication



PHOTONICS



Cryogenic compatibility !

Bay LoCoPack "Concept"



- Product platform designed for automation compatibility from day 1
- Open carrier allows access for P&P machines
- Glass Composite Structure enables new designs to be supplied in low volumes at far lower cost compared to metal packages
- High volumes can also be produced at a low cost
- Reduced development time and faster New
 Product Introduction as same package can be used for prototypes & volume
- Sustainable photonics packaging material
 - Completely transparent package interface offers interesting options for LIDAR



Capillary or molded

2-6 Layer substrates

underfill options

C

Eutectic or lead-free

solder ball options

wire options

Gold, silver or copper

Standardization





In **2010** the PARADIGM (FP7 EU project) partners were taking their first steps to define generic, InP-based, process platforms which could be run in industrial fabs, in an initiative which was unique in the world.

- Some standards exist
 - Low I/O componentry
 - TO, butterfly, DIL
- These were designed many years ago
 - E.g. TO standards 1950s!
- Some "de facto" standards appearing for PIC design
- Clear standards exist for electrical design
- Align with workstation capability







Don't Panic...





Scalable qubits Microsoft is developing hardware, such as this semiconductorsuperconductor heterostructure device, and software for its scalable quantum computer based on topological qubits.

- We understand the need for proof of concept prototypes
- Manual die & wire bonders can be used to break the rules



Contact Details





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Future enabling tech – I/O





- Flip chip
- Cu micropillar
- TSV (through silicon via)
- 2.5D & 3D protocol







I/O per mm² Commercial in confidence